In re Patent Application of
KUMAR ET AL.
Serial No. **10/789,443**
Filed: **FEBRUARY 27, 2004**

In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-3 (canceled).

4. (Previously presented) A memory device comprising:

a flash memory array;

a micro-controller for managing flash memory operations, testing of the device at wafer level and as finished product, redundancy analysis, programming of re-routing cams and validation of the device;

a test mode command interface for coupling with external test equipment;

a circuit block including a register to store a redundancy vector to be programmed in the re-routing cams and the selected paths for programming information, during execution of a cam programming process;

the micro-controller comprising a built-in hardware structure for performing predefined routines of testing, redundancy analysis, programming of re-routing cams and validation of the device internally without exchanging data with the external test equipment, the built-in hardware structure comprising

a first cache memory for storing up to a maximum number N of column addresses of detected failed cells, N being equal to the number of

available column redundancy resources for a sector of the memory array,

an address counter associated with the first cache memory,

an expected data generation circuit for generating expected data,

a data comparison circuit for comparing the generated expected data with data read from a certain memory location pre-programmed with the expected data,

a local data cache defined by a number N of registers equal to the number of column redundancy resources available for each sector of the memory array, each register having a number M of bits coinciding with read parallelism of the memory array, and in which the data comparison circuit writes information relative to the bits on which a failure has occurred,

a bit position counter for bit by bit scanning of the registers of the local data cache,

a second cache memory for storing information relative to detected failed array cells, accessed, in reading and in writing, through a first data bus and controlled through at least one of a second bus from the test mode command interface and a third bus from the micro-controller,

an up/down counter for pointing to one of the registers of the local data cache, to one of the

registers of the first cache memory and to a location of the second cache memory and including a latch for preserving a pointer value,

a cache address generator for generating a current address of the second cache memory based upon a current address in the address counter and the up/down counter, and

a plurality of bus drivers, driven by control signals managed by the micro-controller, for accessing the first data bus and the second cache memory for writing therein the following information

the content of the up/down counter,

information of the position of the detected failed array cells derived from scanning the N registers of the local data cache through the bit position counter,

the column address of columns with detected failed array cells, and

control information stored in the second cache memory through the test mode command interface for executing specific test routines.

5. (Previously presented) The memory device according to Claim 4, wherein the built-in hardware structure of the micro-controller further comprises first and second pointer generators, and a binary adder connected to a multiplexer; wherein the current address in the address counter is provided to the first pointer generator, and the

content of the up/down counter is provided to the second pointer generator, and the data output by the first and second pointer generators is combined by the binary adder coupled to a first input of the multiplexer, a second input of the multiplexer receiving an address of a cache memory location through the test mode command interface, for the selection of an access mode driven by an external command signal through the test mode command interface.

6. (Previously presented) The memory device according to Claim 4, wherein the built-in hardware structure of the micro-controller further comprises a program counter and associated read only memory; and wherein the second cache memory is addressable also through the program counter which provides pointer data to a third input of the multiplexer.

7. (Previously presented) A memory device comprising:

a flash memory array and an associated micro-controller; and

a test mode command interface for coupling the micro-controller with external test equipment;

the micro-controller comprising

a first cache memory for storing column addresses of detected failed cells,

an address counter associated with the first cache memory,

an expected data generation circuit for generating expected data,

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a data comparison circuit for comparing the generated expected data with data read from a certain memory location pre-programmed with the expected data,

a local data cache connected to the data comparison circuit for storing information relative to bits on which a failure has occurred,

a bit position counter for bit by bit scanning of the local data cache,

a second cache memory for storing information relative to detected failed array cells,

an up/down counter for pointing to a location of the local data cache, to a location of the first cache memory and to a location of the second cache memory and including a latch for preserving a pointer value,

a cache address generator for generating a current address of the second cache memory based upon a current address in the address counter and the up/down counter, and

a plurality of drivers for accessing the second cache memory for writing therein the following information

the content of the up/down counter,

information of the position of the detected failed array cells from the local data cache and the bit position counter,

the column address of columns with detected failed array cells, and test control information.

8. (Previously presented) The memory device according to Claim 7, further comprising a repair data generation circuit block associated with the microcontroller, and including a register to store a redundancy vector to be programmed in re-routing cams and the selected paths for programming information, during execution of a cam programming process.

9. (Previously presented) The memory device according to Claim 7, wherein the micro-controller further comprises first and second pointer generators, and a binary adder connected to a multiplexer; wherein the current address in the address counter is provided to the first pointer generator, and the content of the up/down counter is provided to the second pointer generator, and the data output by the first and second pointer generators is combined by the binary adder and coupled to a first input of the multiplexer, a second input of the multiplexer receiving an address of a cache memory location through the test mode command interface, for the selection of an access mode.

10. (Previously presented) The memory device according to Claim 9, wherein the micro-controller further comprises a program counter and an associated read only

memory; and wherein the second cache memory is addressable through the program counter which provides pointer data to a third input of the multiplexer.

Claims 11 and 12 (canceled).

13. (Previously presented) A method of making a memory device comprising:

providing a flash memory array and an associated micro-controller; and

providing a test mode command interface for coupling the micro-controller with external test equipment;

the micro-controller comprising

a first cache memory for storing column addresses of detected failed cells,

an address counter associated with the first cache memory,

an expected data generation circuit for generating expected data,

a data comparison circuit for comparing the generated expected data with data read from a certain memory location pre-programmed with the expected data,

a local data cache connected to the data comparison circuit for storing information relative to bits on which a failure has occurred,

a bit position counter for bit by bit scanning of the local data cache,

a second cache memory for storing information relative to detected failed array cells,

an up/down counter for pointing to a location of the local data cache, to a location of the first cache memory and to a location of the second cache memory and including a latch for preserving a pointer value,

a cache address generator for generating a current address of the second cache memory based upon a current address in the address counter and the up/down counter, and

a plurality of drivers for accessing the second cache memory for writing therein the following information

the content of the up/down counter,

information of the position of the detected failed array cells from the local data cache and the bit position counter,

the column address of columns with detected failed array cells, and

test control information.

14. (Previously presented) The method according to Claim 13, further comprising providing a repair data generation circuit block associated with the microcontroller, and including a register to store a redundancy vector to be programmed in re-routing cams and the selected paths for

programming information, during execution of a cam programming process.

15. (Previously presented) The method according to Claim 13, wherein the micro-controller further comprises first and second pointer generators, and a binary adder connected to a multiplexer; wherein the current address in the address counter is provided to the first pointer generator, and the content of the up/down counter is provided to the second pointer generator, and the data output by the first and second pointer generators is combined by the binary adder and coupled to a first input of the multiplexer, a second input of the multiplexer receiving an address of a cache memory location through the test mode command interface, for the selection of an access mode.

16. (Previously presented) The method according to Claim 15, wherein the micro-controller further comprises a program counter and an associated read only memory; and wherein the second cache memory is addressable through the program counter which provides pointer data to a third input of the multiplexer.